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## AGS+ Hardware Architecture

The AGS+ router was an improved version of the original AGS router. The AGS (without the plus) was based on a Motorola 68000 series CPU (M68k) and used media interface cards interconnected by a relatively slow 155-Mbps data bus called the Multibus. Due to the speed limitations of this processor and the Multibus, packet switching performance was limited to the range of 7000 to 14,000 packets per second (pps) even with fast switching—pretty anemic by today's standards. In fact, under some conditions the Cisco 2500 series routers can outperform these switching speeds!

The Cisco AGS+ and 7000 routers were designed before the advent of high speed computer buses and economical RISC-based CPUs. So, when Cisco's engineers started looking for ways to boost switching performance, there weren't many off-the-shelf solutions from which to choose. The engineers decided to solve the problem by designing their own high-speed data bus and packet switching engine. Thus was born the *Cbus*.

The original Cbus (short for "Cisco bus") was a 32-bit bus operating at 16.67 MHz, giving a total bandwidth of 533 Mbps—a vast improvement over the Multibus. The bus was designed with 32 data lines, 24 address lines, and 8 command lines.

The Cbus switching engine was based on a microcoded 16-bit slice microprocessor with an 80-bit instruction word that allowed several operations to execute concurrently in a single cycle. Unlike general purpose processors such as the M68k, the Cbus processor had a small, customized instruction set designed specifically to support data switching operations. The processor was packaged on a special interface card containing memory for the processor's instructions (called *control store*), fast packet memory, and interfaces to both the Multibus and the Cbus. This card comprised the switching engine and was called the *Cbus Controller*.

These two new features, the Cbus and the Cbus Controller, were added to the original AGS architecture to create the AGS+ router. Figure 4-1 shows a diagram of the AGS+ architecture.

### Figure 4-1. AGS+ Architecture
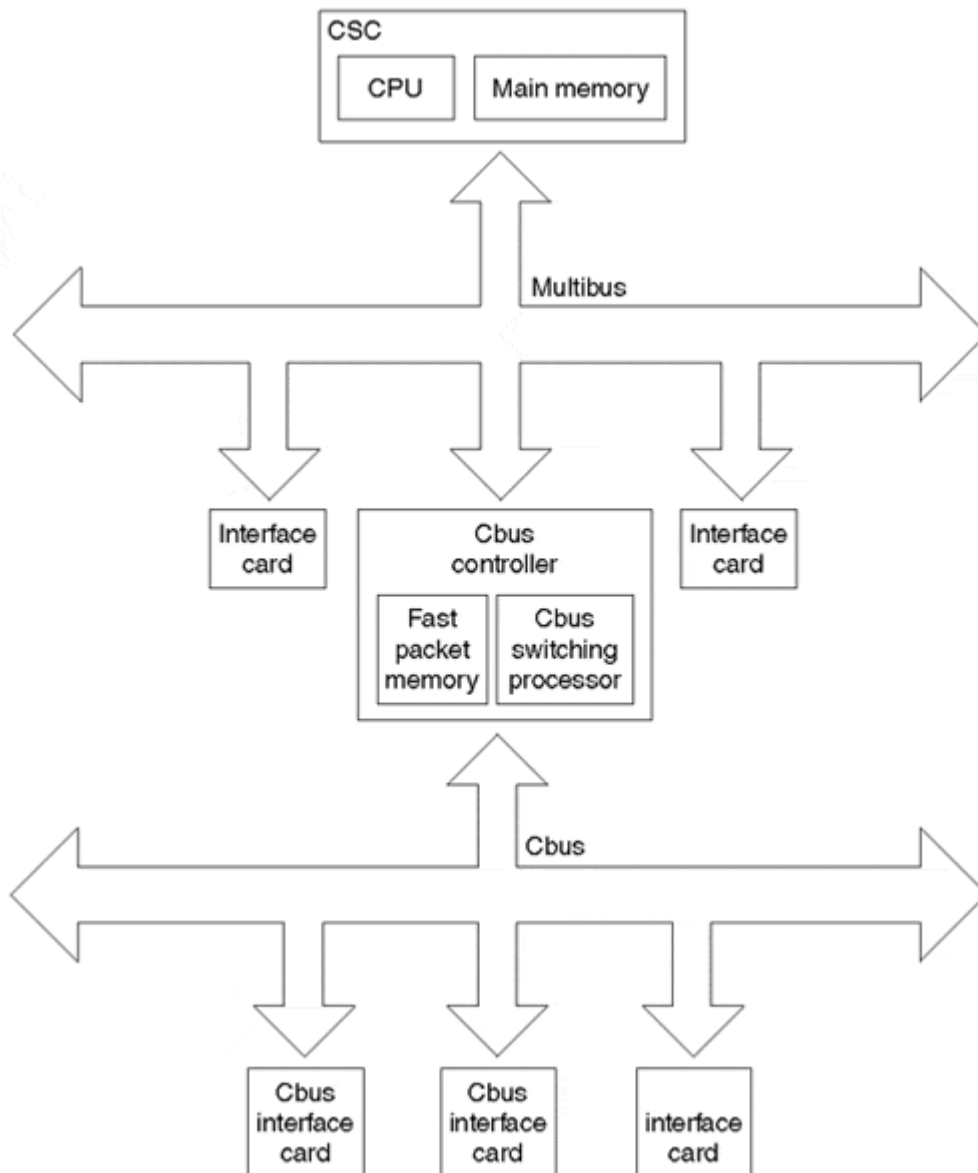
The following list describes each of the major components shown in Figure 4-1:

- **Processor (CPU)—**

  Runs IOS and performs process switching functions, and performs fast switching between Multibus interfaces. The processor also performs fast switching for packets that are received from Cbus interfaces but can't be autonomously switched.

- **Main Memory—**

  DRAM containing the running IOS image, its data, and system packet buffers.

- **Multibus—**

  Data bus interconnecting the processor with the Multibus interface cards. The Cbus controller card also has a connection to the Multibus.

- **Cbus Switching Processor—**

Runs optimized non-IOS microcode to perform fast switching of packets between Cbus interfaces. This processor is on the Cbus controller card.

- **Fast Packet Memory—**

  High-speed memory on the Cbus controller card that is dual-ported between the Cbus switching processor and the Cbus interface cards. Used to store packets received from or transmitted to Cbus interfaces. This memory is referred to by the name *MEMD* in the Cbus architecture.

- **Cbus—**

  The Cisco proprietary data bus interconnecting the Cbus controller card with the Cbus interface cards.

  **NOTE**

  The Cbus processor, MEMD, and Cbus bus control circuitry were contained on the same card and collectively referred to as the CBUS controller or CBUSII card. The Cbus processor itself was often just referred to as "the processor on the CBUSII card." *Cbus Switching Processor* is used here to identify the processor and should not be confused with the *Switch Processor* on the C7000 router.

The AGS+ retained the Motorola 68000 series processor and the Multibus backplane used on the AGS. The Cbus enhancement was made by converting five of the interface card slots on the backplane to access the Cbus. This allowed Multibus interface cards to be used in the same chassis with the new Cbus interface cards.

After the hardware enhancements were added to the AGS+, how did IOS actually use them to increase switching performance? Let's examine how IOS put these enhancements to work.

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